

Fig. 1

FIG. 2 is a block diagram of a system 200 for wafer processing. The system 200 includes a wafer source 210, an RTA process chamber 220, an R_s measurement chamber 230, a feedback generator 250, a data store 260, and a wafer destination 240. The wafer source 210 is connected to the RTA process chamber 220. The RTA process chamber 220 is connected to the R_s measurement chamber 230. The R_s measurement chamber 230 is connected to the feedback generator 250. The feedback generator 250 is connected to the data store 260. The data store 260 is connected to the wafer source 210. The RTA process chamber 220 is also connected to the feedback generator 250. The feedback generator 250 is connected to the R_s measurement chamber 230. The R_s measurement chamber 230 is connected to the wafer destination 240.

200

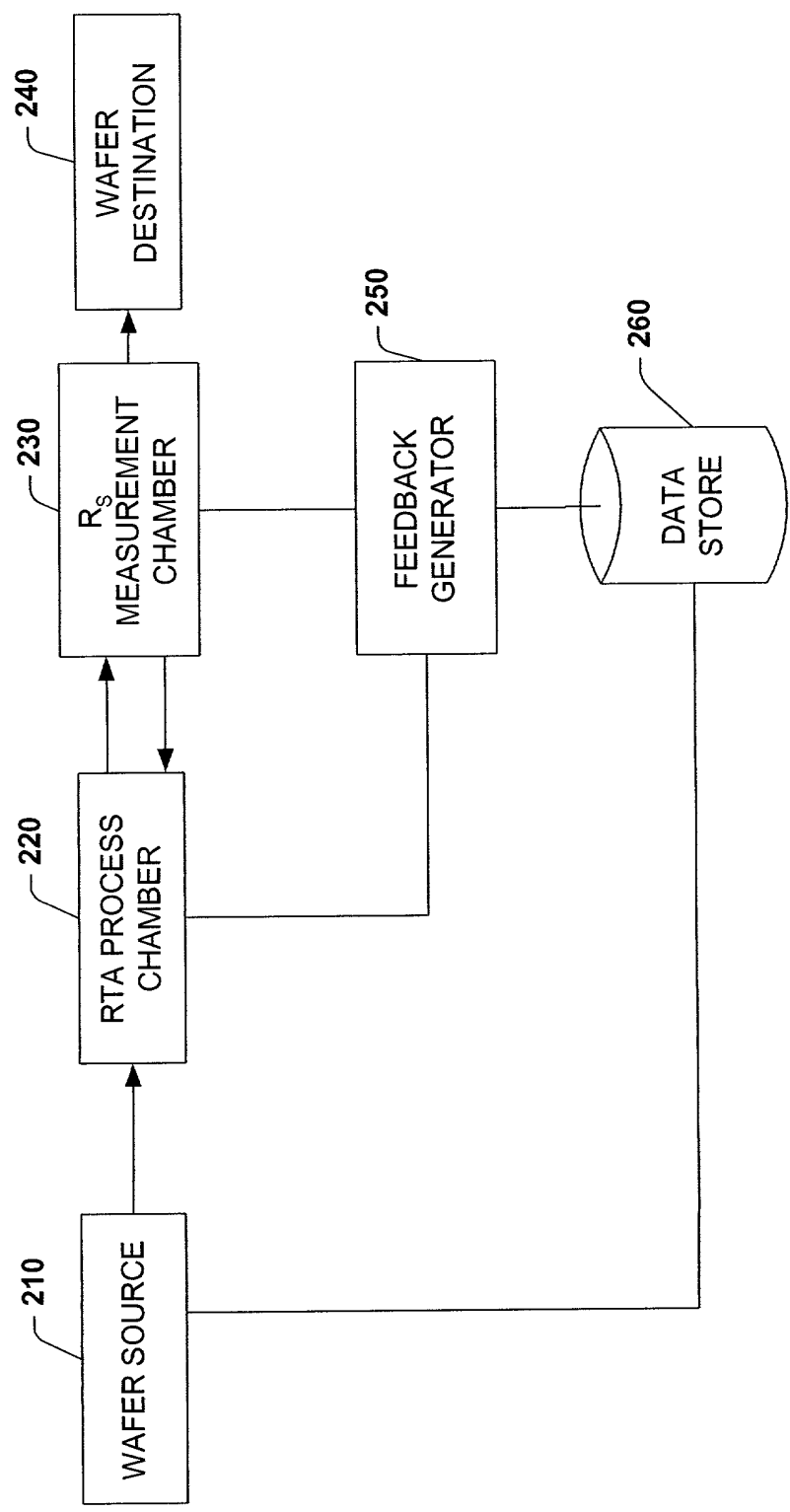


Fig. 2

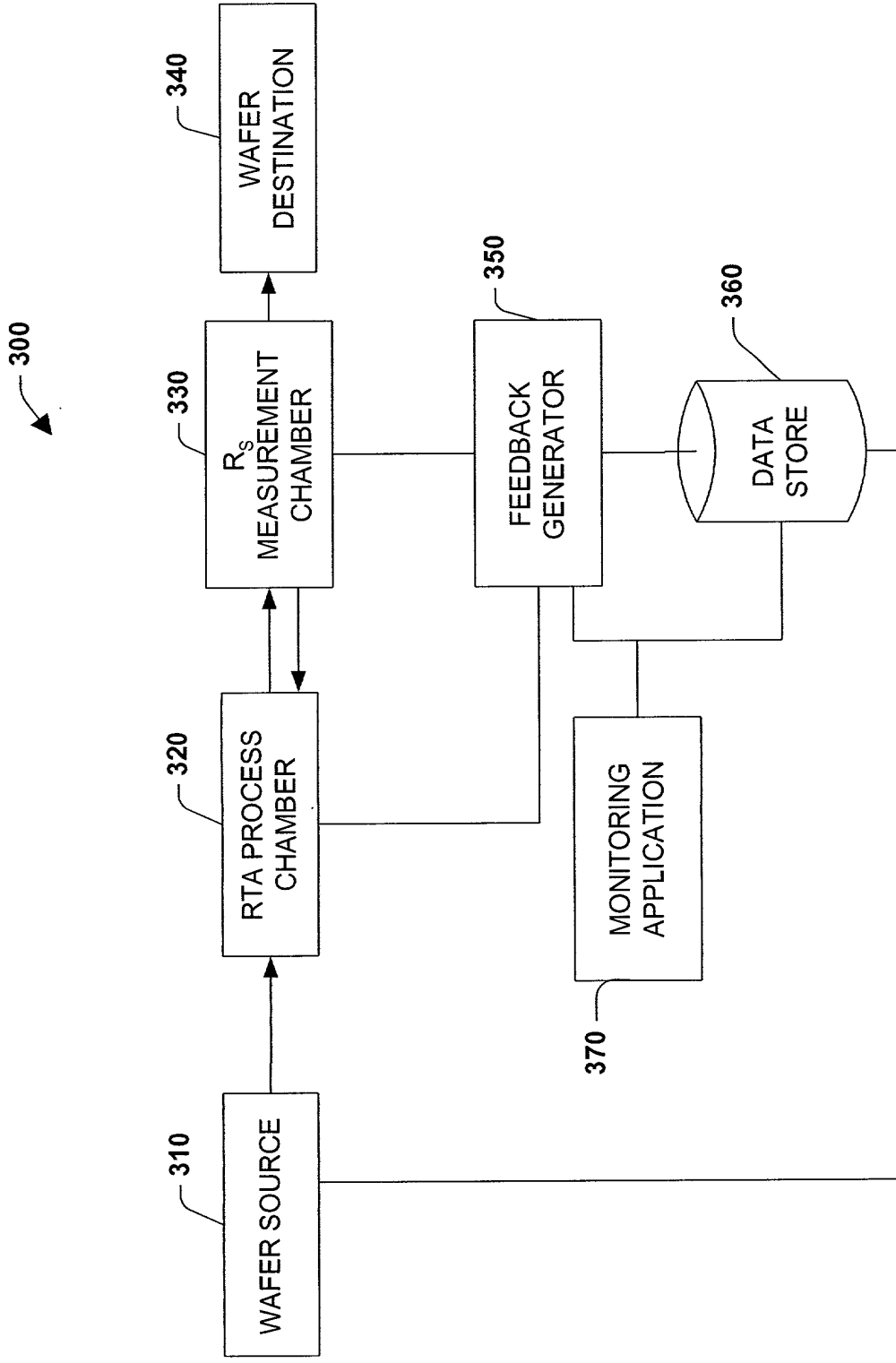


Fig. 3

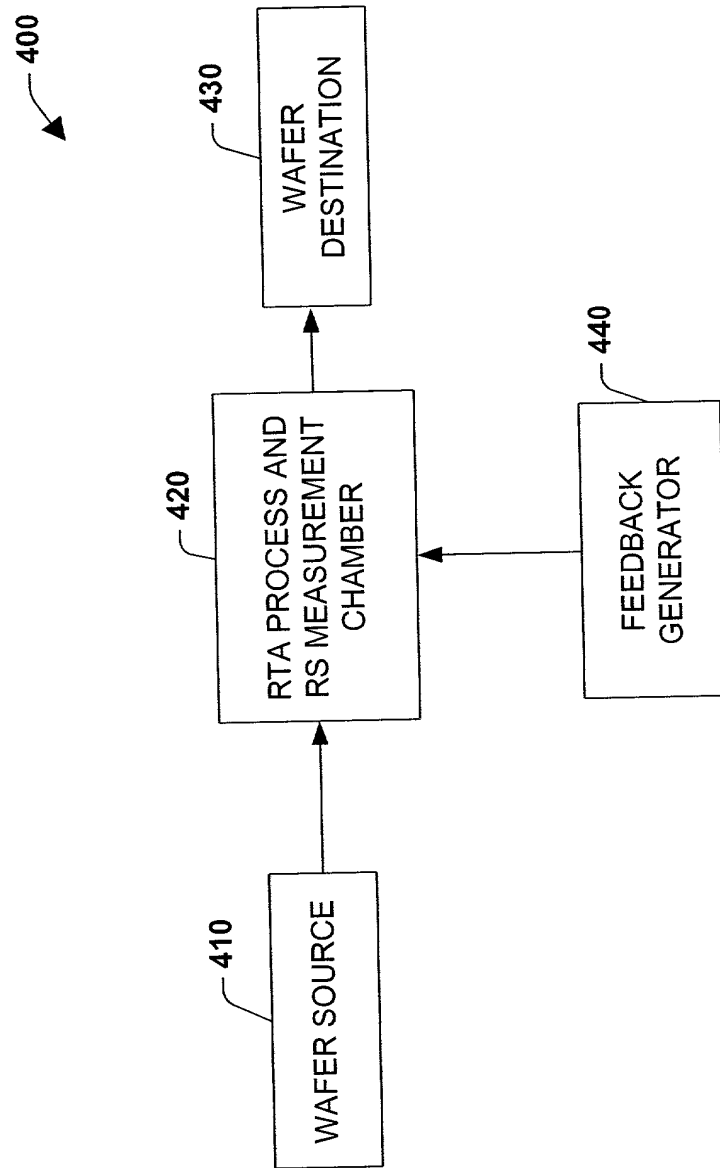


Fig. 4

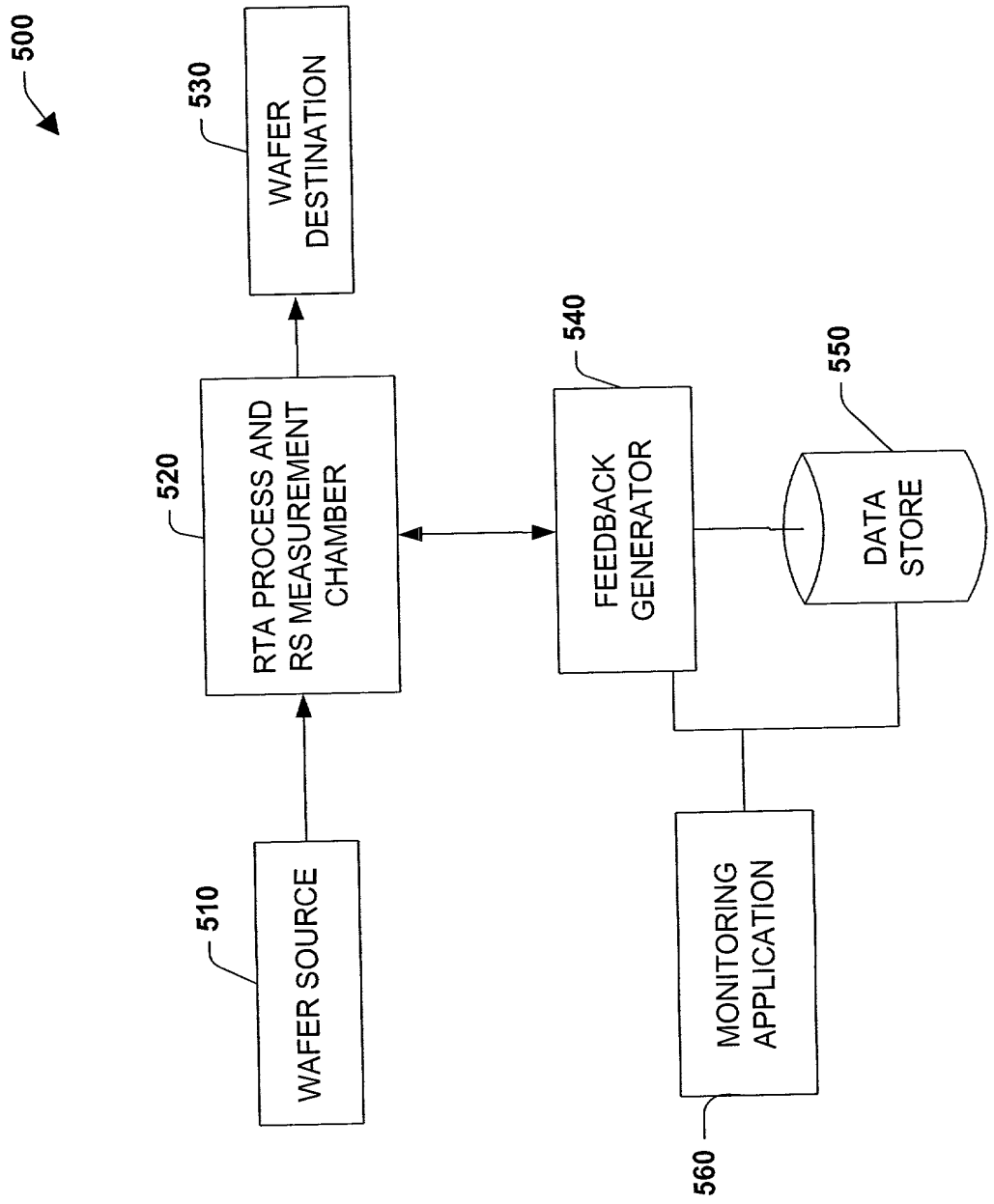


Fig. 5

FIG. 6 is a perspective view of a device 20. The device 20 includes a substrate 22 and a layer 24 disposed on the substrate 22. The layer 24 is a thin layer of material disposed on the substrate 22. The layer 24 is a thin layer of material disposed on the substrate 22. The layer 24 is a thin layer of material disposed on the substrate 22.

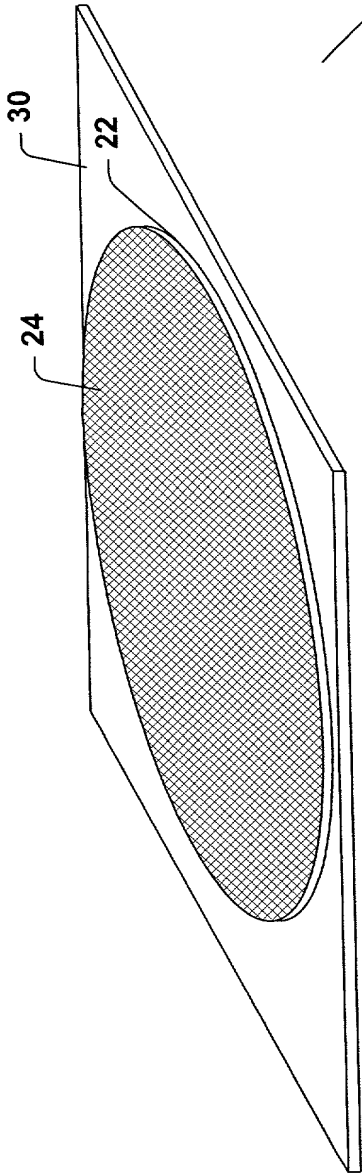


Fig. 6

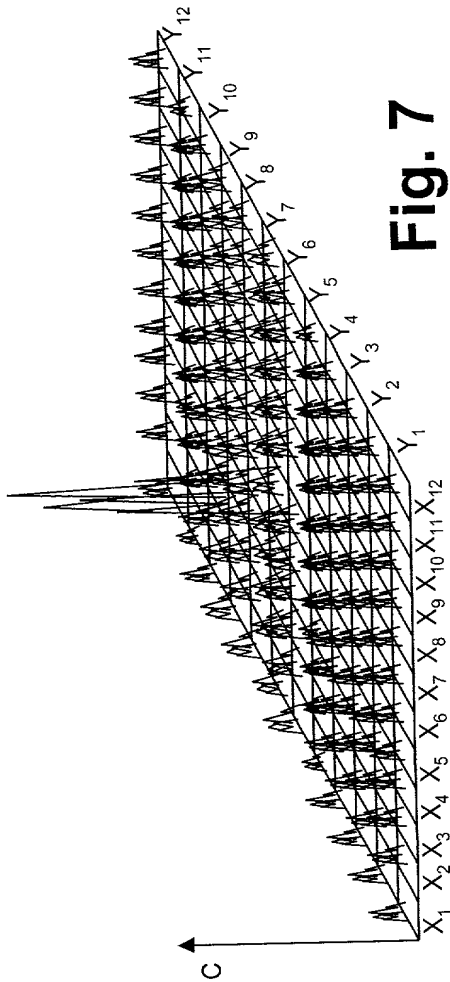


Fig. 7

	X ₁	X ₂	X ₃	X ₄	X ₅	X ₆	X ₇	X ₈	X ₉	X ₁₀	X ₁₁	X ₁₂
Y ₁	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A
Y ₂	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A
Y ₃	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A
Y ₄	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A
Y ₅	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A
Y ₆	T _A	T _A	T _A	T _A	T _A	T _A	T _U	T _A	T _A	T _A	T _A	T _A
Y ₇	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A
Y ₈	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A
Y ₉	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A
Y ₁₀	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A
Y ₁₁	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A
Y ₁₂	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A	T _A

Fig. 8

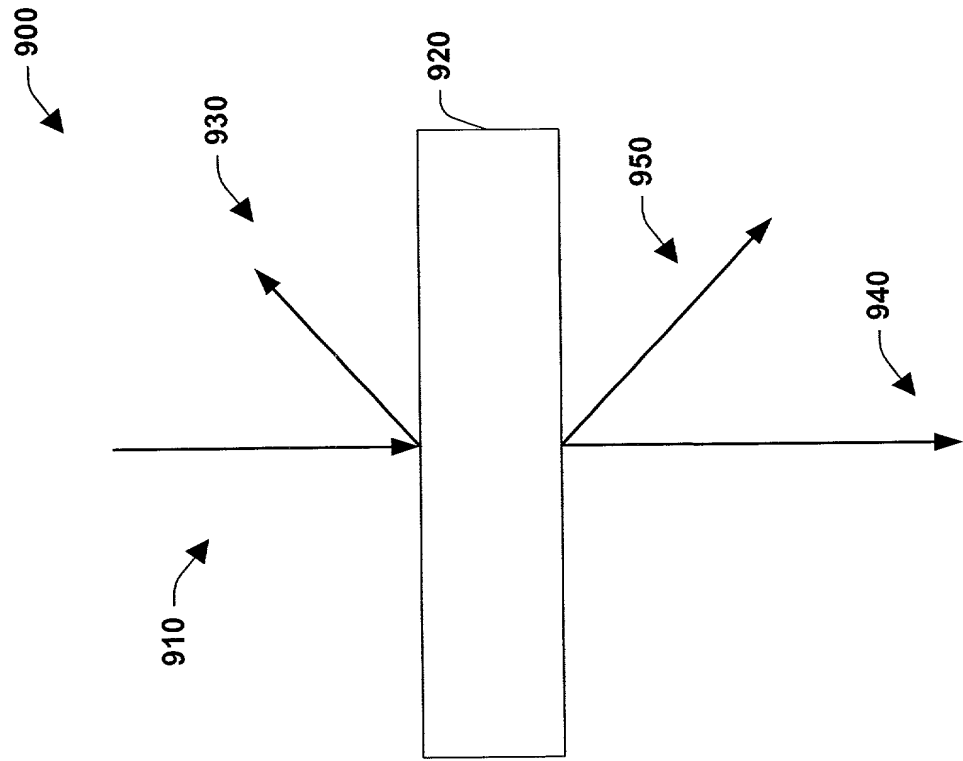


FIG. 9

FIG. 10 is a schematic diagram of a device 1000, which is a cross-sectional view of a device 1000. The device 1000 includes a substrate 1010, a gate stack 1020, a gate stack 1030, a gate stack 1040, and a gate stack 1050. The gate stack 1020 is located on the substrate 1010, and the gate stack 1030, 1040, and 1050 are located on the gate stack 1020. The gate stack 1030, 1040, and 1050 are arranged in a row, and the gate stack 1030 is located between the gate stack 1040 and the gate stack 1050. The gate stack 1030, 1040, and 1050 are arranged in a row, and the gate stack 1030 is located between the gate stack 1040 and the gate stack 1050.

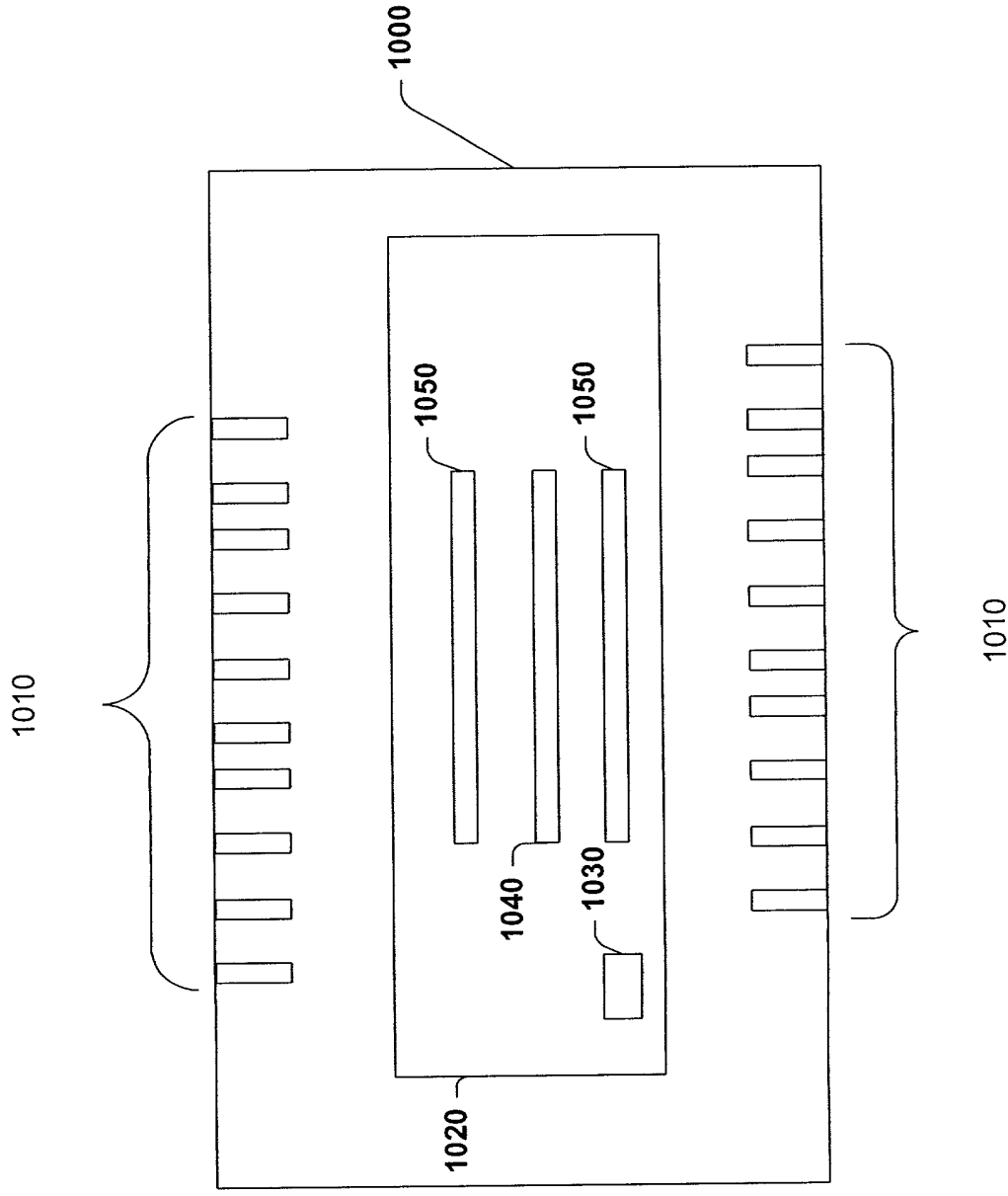


FIG. 10

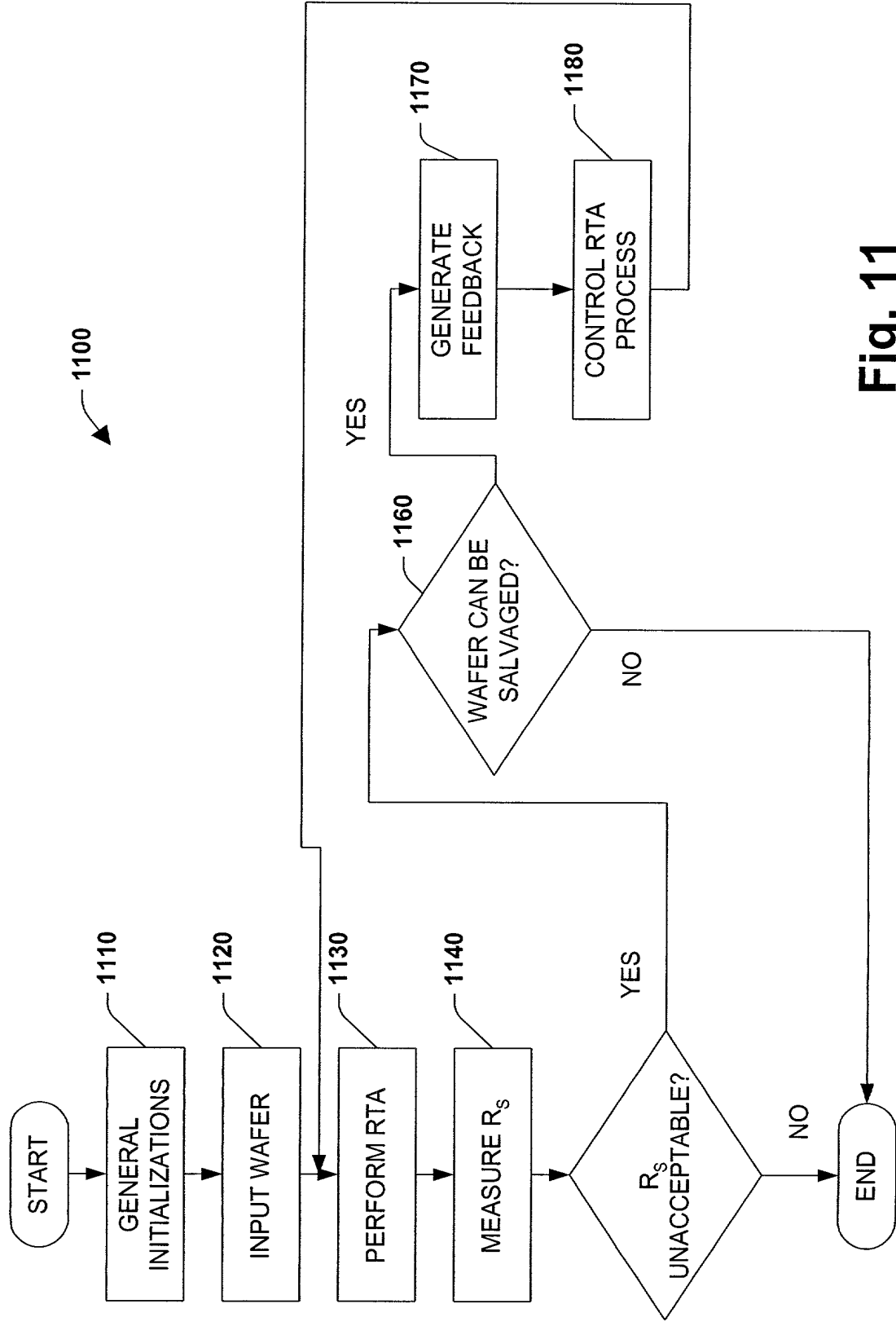


Fig. 11

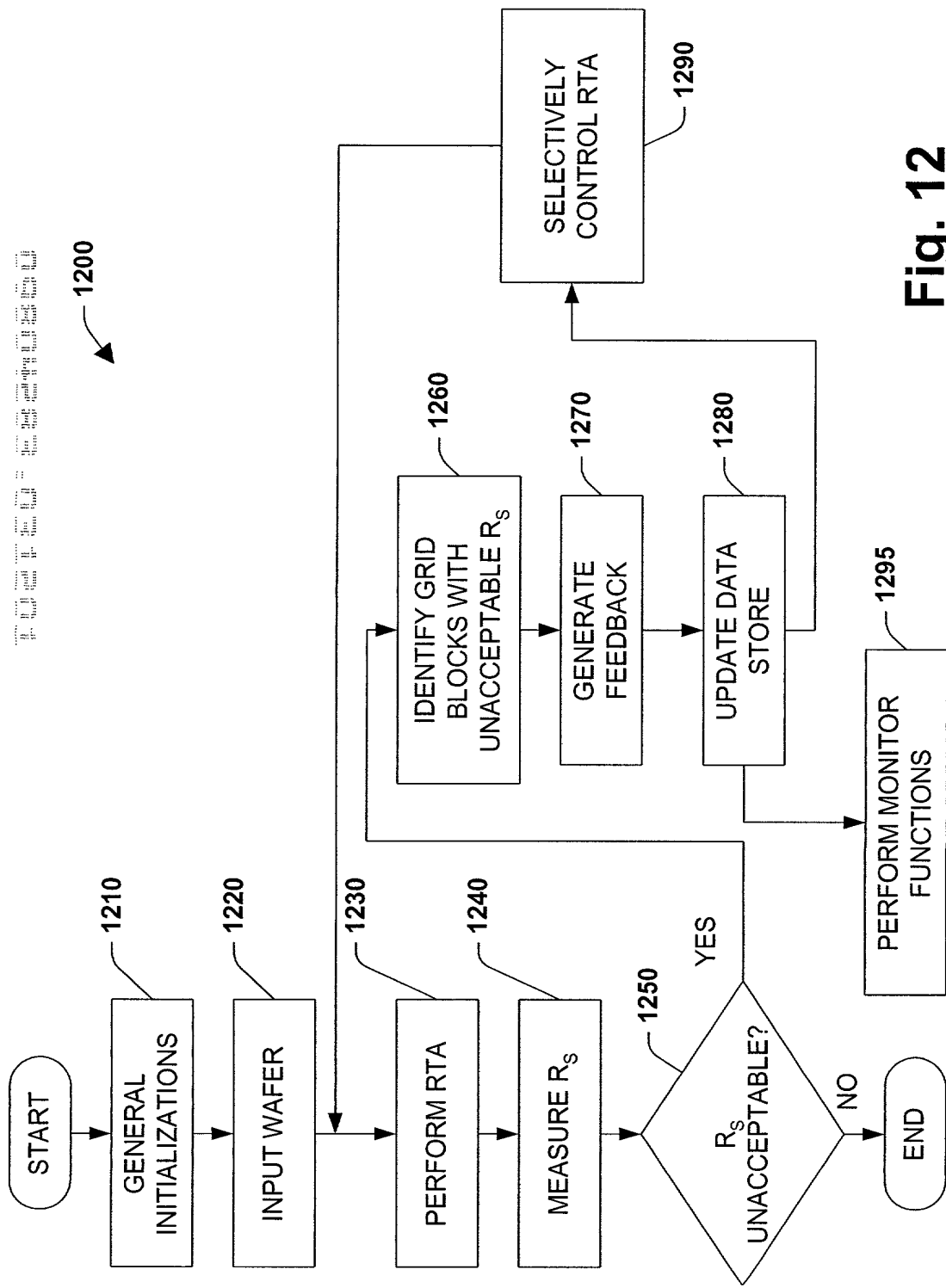


Fig. 12